IN THE SPECIFICATION

On page 4, please replace the paragraph beginning on line 16 with the following amended paragraph:

The receiver employs a multi-phase clock generator that runs plesiochronously with respect to the transmit clock. A frequency difference between the two clock bases is specified to be less than a few hundreds parts per millions. The receiver functionality is divided into three main sections, i.e., an edge detector section, an edge processing section and an elastic buffer section. A high-level block diagram of this illustrative structure is shown in FIG 2, which depicts edge buffer 22, edge processing section 24, and multi-phase clock generator 28~~26~~.

On page 11, please replace the paragraph beginning on line 3 with the following amended paragraph:

FIG 6 depicts an exemplary embodiment of a method ~~60~~ according to one aspect of the invention. According to this embodiment, the transmitted clock is tracked with multiple locally-generated clock phases (step 71). The average phase of the detected edges is estimated (step 72). A pulse edge in the data stream is registered at the transition phase corresponding to one of the multiple locally-generated clock phases (step 73). Next, it is determined whether the first symbol was received multiple times consecutively (step 74). This determination is then used in the receiver decision process (step 75).